58. (Amended) A system comprising:
a central processing unit with associated register file; and
a hardware accelerator operably connected to the central processing unit, the hardware accelerator adapted to convert stack-based instructions into register-based instructions native to the central processing unit, where the hardware accelerator increments the Java PC within the hardware accelerator by generating an increment value based on the number of byte codes being disposed, wherein the Java PC is incremented in the correct manner if multiple bytecodes are disposed at the same time .

Please add new Claims 60-62 as follows:

60. (New) The system of claim 1, wherein the indication of the order of the instructions is the native program counter value.

61. (New) The system of claim 31, wherein if the stack depth is above the maximum depth an overflow flag is generated.

62. (New) The system of claim 31, wherein if the stack depth is below the minimum depth an underflow flag is generated.